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EXAMINER

RIZK, SAMIR WADIE

ART UNIT

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2112

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/706,187	Applicant(s) KIM ET AL.	
	Examiner SAM RIZK	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date | 6) <input type="checkbox"/> Other: _____ |

11/12/2003, 3/1/2004, 5/20/2004, 7/19/2004, 8/13/2004, 11/5/2004, 4/1/2005, 7/28/2005, 10/17/2005, 2/13/2006, 6/19/2006, 8/21/2006, 4/17/2008.

DETAILED ACTIONS

- Claims 1-20 have been submitted for examination
- Claims 1–20 have been rejected

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ushirokawa et al. US patent no. 5621764 (Hereinafter Ushirokawa).
2. In regard to claim 1, Ushirokawa teaches:
 - A decoding unit for decoding a received signal comprising:
 - a plurality of soft-decoders, each soft-decoder sampling the received signal at a different time within a symbol period and outputting two values, the first value comprising a preliminary decoded value and the second value comprising an ambiguity indicator; and
(Figure 9, ref. (41₁ to 41_k) in Ushirokawa)
 - a logic device coupled to the each of the soft-decoders, for determining a decoded value for each symbol based on one or more preliminary decoded values and ambiguity indicators.

Art Unit: 2112

(Figure 9, ref. 12 in Ushirokawa wherein the soft decision is based on the hard decision and the reliability information (i.e. ambiguity indicator(s))

3. In regard to claim 2, Ushirokawa teaches:

- The decoding-unit of Claim 1, wherein each of the soft-decoders are identical.

(Figure 9, ref. (41₁ to 41_k) in Ushirokawa)

4. In regard to claim 3, Ushirokawa teaches:

- The decoding unit of Claim 1, wherein each soft-decoder comprises:
- a first comparator with inputs comprising the received signal and a first reference voltage;

(Figure 10, ref. (43₁ to 43_k) wherein the threshold level (can be a voltage reference (level)) is set as per figure 11 in Ushirokawa)

- a second comparator with inputs comprising the received signal and a second reference voltage; and

(Figure 10(a), ref. (43₁ to 43_k) wherein the threshold level (can be a voltage reference (level)) is set as per figure 11 in Ushirokawa)

- a third comparator with inputs comprising the received signal and a third reference voltage.

(Figure 10, ref. (43₁ to 43_k) wherein the threshold level (can be a voltage reference (level)) is set as per figure 11 in Ushirokawa)

5. In regard to claim 4, Ushirokawa teaches:

- The decoding unit of Claim 1, wherein each soft-decoder comprises a plurality of comparators and one or more logical AND gates.

(Figure 10(a), ref 45 in Ushirokawa)

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Ramanujam et al. US patent no. 7340185 (Hereinafter Ramanujam).
7. In regard to claim 11, Ramanujam teaches:
 - A decoding unit for decoding a received signal comprising:
an analog-to-digital converter for sampling the received signal faster than once every symbol period of the received signal;
(Figure 2, ref. (203) in Ramanujam)
 - a processor coupled to the converter for grouping a subset of sampled values derived from the single symbol period, for examining the subset of values and determining a value closest to an optimum sampling time based on a principle of generalized maximum likelihood, for decoding the value closest to the optimum sampling time and outputting that sample as the decoded symbol.

Art Unit: 2112

(Figure 1, ref. (110) & (112) and col. 1, lines (50-57) in Ramanujam)

8. In regard to claim 12;

- The decoding unit of Claim 11, further comprising a clock recovery unit coupled to the converter for providing a clock signal.

A person skilled in the art would recognize that clock recovery function is inherent in providing the clock signal for any optical receiver(s).

9. In regard to claim 13, Ramanujam teaches:

- The decoding unit of Claim 11, wherein the processor calculates the value closest to the optimum sampling time by:
- computing an absolute difference between each value and a nearest level corresponding to a decoded symbol finding a value which has a smallest absolute difference from the subset of values; and
- taking the sample with the smallest absolute difference as the sample closest to the optimum sampling time.

(col. 3, lines (19-32) in Ramanujam)

10. Claim 14 is rejected for the same reasons as per claim 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2112

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
11. Claims 5-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ushirokawa as applied to claim 1 above, and further in view of Ramanujam et al. US patent no. 7340185 (Hereinafter Ramanujam).
12. In regard to claim 5, Ushirokawa teaches substantially all the limitations in Claim 1.

However, Ushirokawa does not teach:

- The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders.

Ramanujam in an analogous art that teach optical signal receiver with dual stage soft detection teaches;

- The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders.

(Figure 1, ref. (110) and (112) and figure 2, ref. (204) and figure 3, ref. (304-1 through 304-N) and col. 3, lines (1-10) and (lines (55-67) through col. 4, lines (1-8) in Ramanujam)

Art Unit: 2112

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Ushirokawa with the teaching of Ramanujam to include the coupling of delay elements with the soft-decision decoders.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to for accurate and reliable detection on the Giga bit optical receiver systems.

13. In regard to claim 6, Ramanujam teaches:

- The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying the received signal by a different amount.

(Figure 1, ref. (110) and (112) and figure 2, ref. (204) and figure 3, ref. (304-1 through 304-N) and col. 3, lines (1-10) and (lines (55-67) through col. 4, lines (1-8) in Ramanujam)

14. In regard to claim 7, Ramanujam teaches:

- The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying the clock signal by a different amount.

(Figure 1, ref. (110) and (112) and figure 2, ref. (204) and figure 3, ref. (304-1 through 304-N) and col. 3, lines (1-10) and (lines (55-67) through col. 4, lines (1-8) in Ramanujam)

Art Unit: 2112

15. In regard to claim 8, Ramanujam / Ushirokawa teaches:

- A decoding unit for decoding a received signal comprising:
- an asynchronous soft-decoder that continuously samples the received signal;
(col. 3, lines (3-10) in Ramanujam)
- a plurality of first delay elements coupled to a first soft-decoder, each first delay element generating a different delay relative to another first delay element and producing a first ambiguity indicator;
(Figure 2, ref. (204) and col. 3, lines (3-10) in Ramanujam)
- a plurality of second delay elements coupled to a second soft-decoder output, each second delay element generating a different delay relative to another second delay element and producing a preliminary decoded output; and
(Figure 2, ref. (204) and col. 3, lines (3-10) and lines (19-31) in Ramanujam)
- a logic device coupled to the each of the delay elements, for determining a decoded value based on one or more the preliminary decoded output and ambiguity indicators.

(Figure 9, ref. 12 in Ushirokawa wherein the soft decision is based on the hard decision and the reliability information (i.e. ambiguity indicator(s))

16. In regard to claim 9, Ramanujam / Ushirokawa teach:

- The decoding unit of Claim 8, wherein the soft-decoder comprises:
- a first comparator with inputs comprising the received signal and a first reference voltage;

Art Unit: 2112

- a second comparator with inputs comprising the received signal and a second reference voltage; and
- a third comparator with inputs comprising the received signal and a third reference voltage.

(Figure 10, ref. (43₁ to 43_k) wherein the threshold level (can be a voltage reference (level)) is set as per figure 11 in Ushirokawa) and (figure 2, ref (208) in Ramanujam)

17. Claim 10 is rejected for the same reasons as per claim 4.

18. In regard to claim 15, Ushirokawa teaches:

- The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises generating an ambiguity indicator and a preliminary decoded value for a sample.

(Figure 9, ref. (41₁ to 41_k) in Ushirokawa)

19. Claim 16 is rejected for the same reasons as per claim 6.

20. In regard to claim 17, Ushirokawa/Ramanujam teach:

- The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:
- dividing an ambiguity indicator signal and a preliminary decoded value signal derived from the received signal; and
- delaying each ambiguity indicator signal and each preliminary decoded value signal by different amounts of time.

Art Unit: 2112

(Figure 9, ref. 12 in Ushirokawa wherein the soft decision is based on the hard decision and the reliability information (i.e. ambiguity indicator(s) and figure 2, ref. (204) in Ramanujam)

21. Claim 18 is rejected for the same reasons as per claim 9.
22. Claim 19 is rejected for the same reasons as per claim 11.
23. Claim 20 is rejected for the same reasons as per claim 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Art Unit: 2112

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

/Sam Rizk/

Primary Examiner, Art Unit 2112